Transporter Based Common Mode Voltage Control Techniques in Three-Level Diode-Clamped Inverter

Md. Javed Akhtar[1],and Rohit Gedam[2]

[1]Electrical & Electronics Engineering Department, RKDF University, Bhopal, M.P, India
[2] Electrical & Electronics Engineering Department, RKDF University, Bhopal, M.P, India
[1]javedakhtar338@gmail.com , [2]rohitgrdam92@gmail.com

* Corresponding Author: Author Name Manuscript Received: Manuscript Accepted:

Abstract: *Exchanging converters are utilized in electric drive applications to create variable voltage, variable recurrence supply which produces unsafe enormous dv/dt and high-recurrence basic mode voltages (CMV). Staggered inverters create lower CMV when contrasted with customary two-level inverters. This paper presents straightforward transporter based strategy to control the normal mode voltages in staggered inverters utilizing various structures of sine-triangle examination technique, for example, stage air (PD), stage resistance mien (POD) by adding regular mode voltage balance sign to real reference voltage signal. This paper likewise introduced the strategy to streamline the greatness of this counterbalance sign to diminish CMV and complete consonant bending in inverter yield voltage. The introduced strategies give equivalent execution as acquired in complex space vector-based control methodology, as far as number of recompenses, greatness, and pace of progress of CMV and consonant profile of inverter yield voltage. Reproduction and test results introduced affirm the adequacy of the proposed strategies to control the regular mode voltages.*

Keywords: *CMV, PD, POD, NPC, ASD, PLECS*

1. Introduction

In the medium-voltage, high-power adjustable speed drive (ASD) system, AC supply is first converted into DC (known as DC buffer stage) and then converting back this DC into variable voltage variable frequency AC supply using inverter (voltage source or current source type). Figure 1 shows the general block diagram of AC-DC-AC induction motor drive system. The front-end converter may be uncontrolled or controlled voltage source or current source rectifier while the motor side converter can be conventional two-level or multilevel VSI, CSI. In VSI fed drive, the DC link capacitor (and) is sufficiently large and DC link inductor is not required whereas in CSI fed drive, is sufficiently large and is not needed [1, 2].

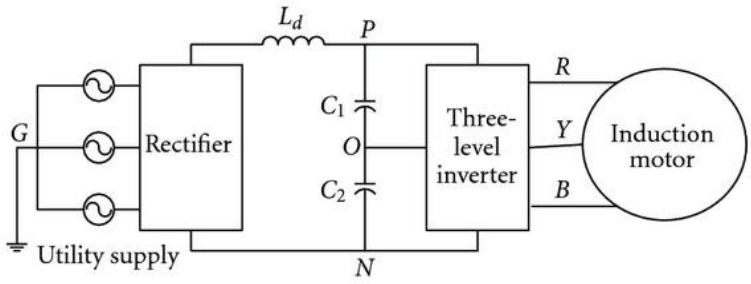

Figure 1. General block diagram of AC-DC-AC VSI or CSI fed ASD (only L_d in CSI and only C_1, C_2 in VSI).

2. Common Mode Voltage Control

Various common mode voltage reduction/elimination techniques can be classified as given below.

(A) Using some extra hardware circuitry such as

(i) isolation transformer;

(ii) zero-sequence impedance (common mode choke);

(iii) active and passive filters;

(iv) dual bridge inverter;

(v) using four-leg (four-phase) inverter.

(B) Using modification in control strategy employed such as, based on

(i) space vector PWM technique (SVPWM);

(ii) sinusoidal PWM technique (SPWM).

The proper choice of common mode choke provides high impedance to common mode current and can eliminate the CMV. Further, any practice to eliminate CMV may increase the common mode current [9, 11]. Thus, investigation is required on this issue. The main issue is that the THD and switching losses increase with controlling the CMV. During the control pulse generation in multilevel inverters, some switching states produce reduced/zero common mode voltage across motor windings and inverter output terminals.

In SVPWM techniques, the switching state voltage vectors generating zero common mode voltage are only used [7, 8]. Various forms of SVPWM techniques are available to mitigate the common mode voltage problem, that is, nearest three vector selection (NTV) SVPWM, radial state SVPWM, zero common mode voltage SVPWM, and so forth [8].

In ASD system, magnitude and rate of change of CMV play an important role in designing EMI filters. SVPWM-based techniques for this purpose require comparatively complex algorithm [7, 9–12]. On the other hand, SPWM-based techniques require less complex algorithm with ease to implement.

This section presents various simple SPWM-based techniques controlling the magnitude and rate of change of CMV. Different SPWM techniques can be classified as [14–16]

(i) Phase disposition (PD) method,

(ii) Phase opposition Disposition (POD) method,

(iii) Phase-shifted (PS) method,

(iv) Hybrid (H) method,

(iv) Third harmonic injection (THIPWM) method.

3. Simulation And Experimental Results

3.1 Three-Level Spwm Techniques

The PLECS Blockset is an add-on to the MatLab/Simulink software program that was designed for the efficient simulation of power electronic systems. This is achieved by treating the switching behavior of the power semiconductors as ideal switches, with equivalent series resistances and inductances to obtain accurate on-state voltage drops and rise/fall times of the output currents. The PLECS program also offers the ability to perform thermal analysis of the power semiconductors. This is accomplished through the use of lookup tables generated from device datasheets with respect to the device's current-voltage (I-V) curve, conduction and switching loss curves, and thermal parameters.

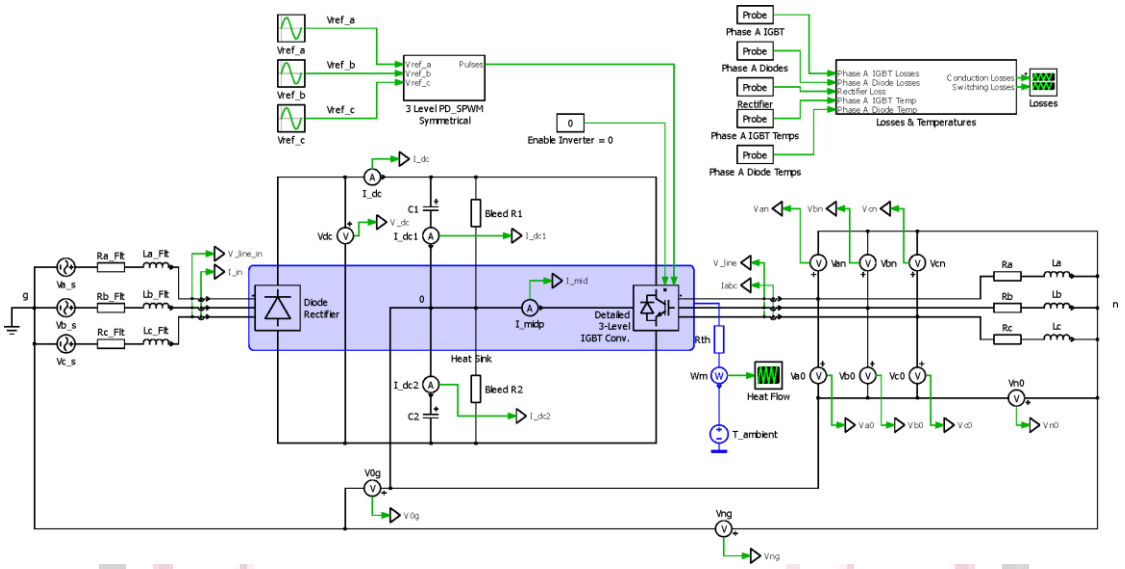

Figure 3.1: three-level NPC ASD modeled in the PLECS Blockset program.

A similar model was developed in MatLab/Simulink for shaft voltage and bearing current analyses of the three SPWM algorithms, which is shown in Figure 3.2. Custom subsystems were developed for the three phase rectifier, dc bus, three-level NPC VSI, PWM algorithm, CM equivalent PWM inverter-fed motor model, and circuit measurements.

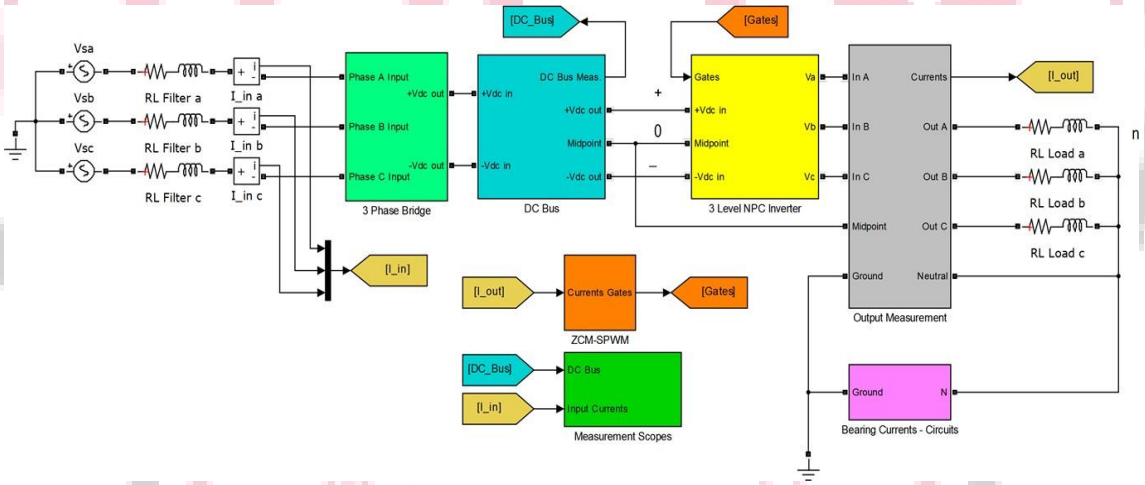

Figure 3.2: Three-level NPC ASD modeled in the MatLab / Simulink program.

TABLE 3.1: SIMULATION PARAMETERS OF THE THREE-LEVEL NPC ASD.

Simulation Parameters	Value	Units
PWM factor	0.628	
SFO zero sequence injection	Yes	
Carrier frequency	2	kHz
Reference frequency	60	Hz
IGBT dead-time	6	µs

Table 4.2: circuit parameters for simulation of the three-level NPC ASD.

Circuit Parameters	Value	Units	Circuit Parameters	Value	Units
Source voltage (L-L)	208	V	dc bus capacitor C1	3.5	mF
Source frequency	60	Hz	dc bus capacitor C2	3.5	mF
Input filter inductance	1.5	mH	Load inductance	250	mH
Input filter resistance	18	mΩ	Load resistance	20	Ω

As predicted in the theoretical development and illustrated in Figure 3.3, the simulated *vn*0 CMV using the PD-SPWM technique takes on values of ± 13 V_{dc}, ± 16 V_{dc}, and 0 V_{dc}, which validates the use of 25 of the 27 three-level switching states.

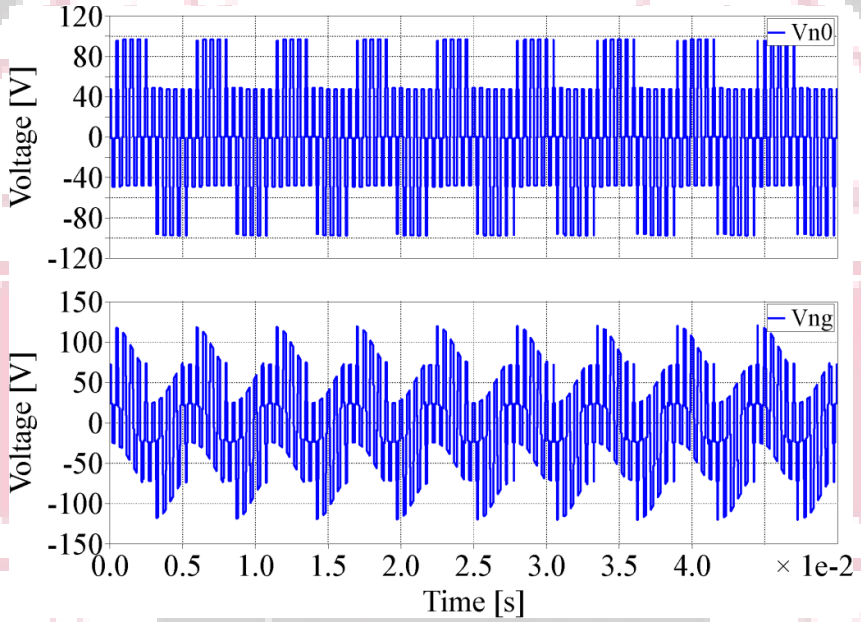

Figure 3.3: Simulated time-domain waveforms of load neutral to dc bus midpoint CMV (top) and load neutral to frame ground CMV (bottom) using PD-SPWM.

The associated simulated FFT waveform, see Figure 3.4, indicates that the majority of the harmonic spectra occur near the carrier frequency of 2 kHz.

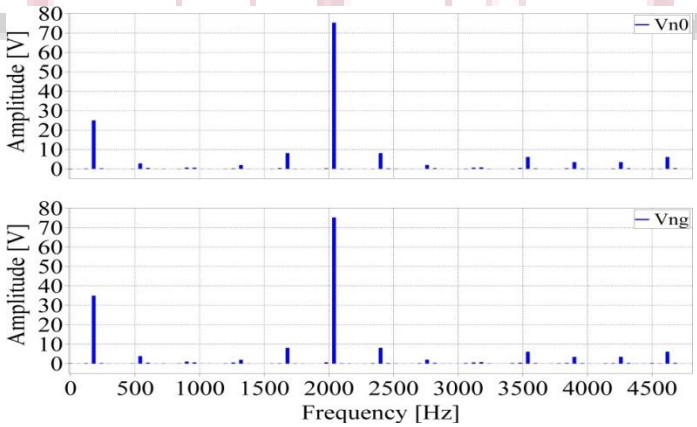

Figure 3.4: FFT of simulated load neutral to dc bus midpoint CMV (top) and load neutral to frame ground CMV (bottom) using PD-SPWM.

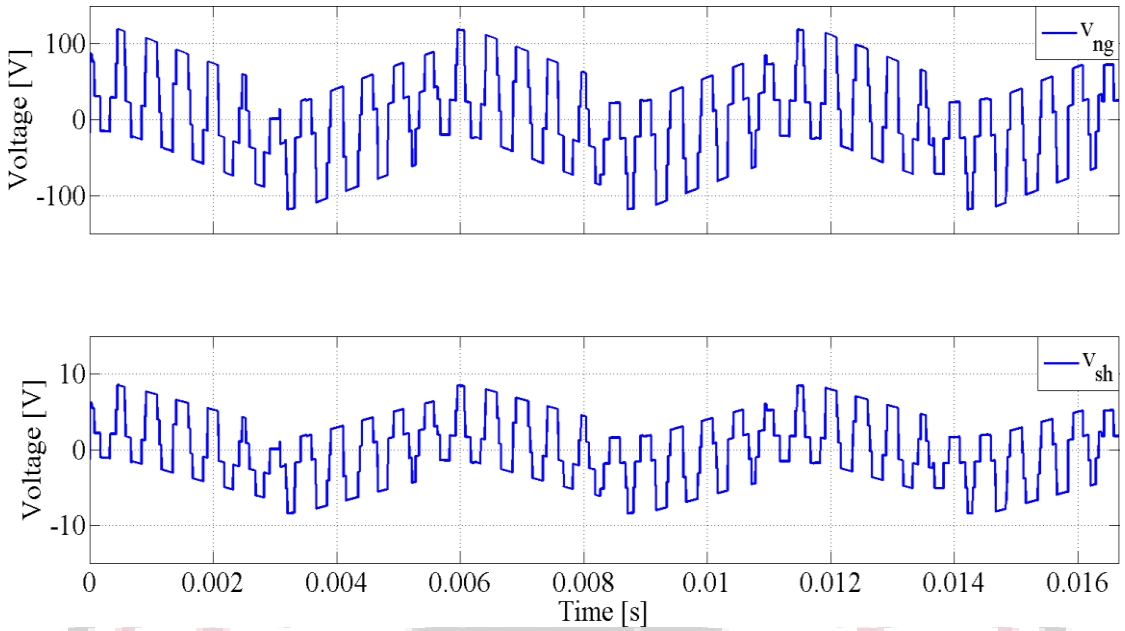

Figure 3.4 : simulated time-domain waveforms of load neutral to frame ground CMV (top) and shaft voltage (bottom) using PD-SPWM.

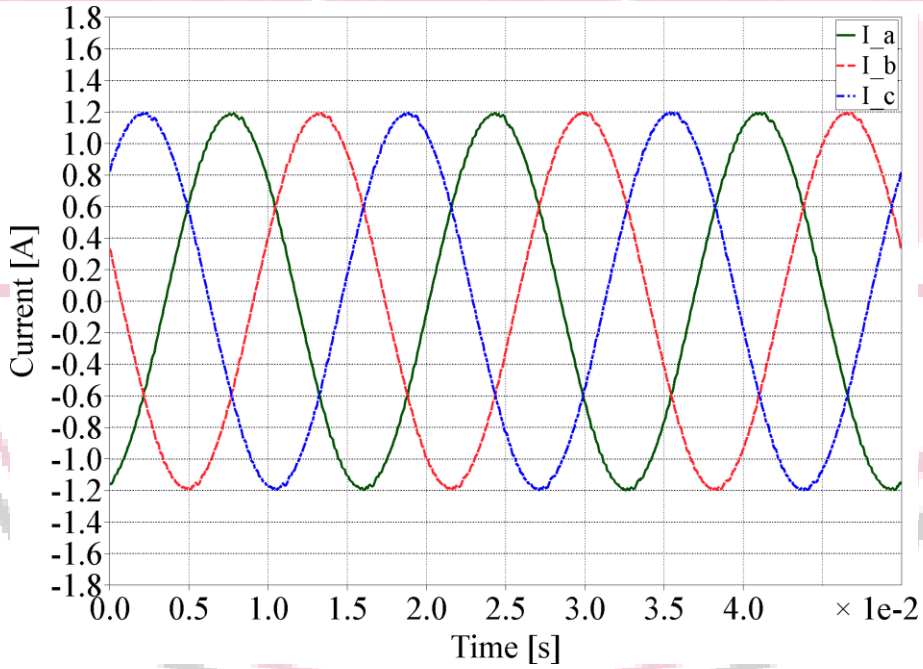

Figure 3.5: simulated time-domain waveforms of output line currents using PD- SPWM.

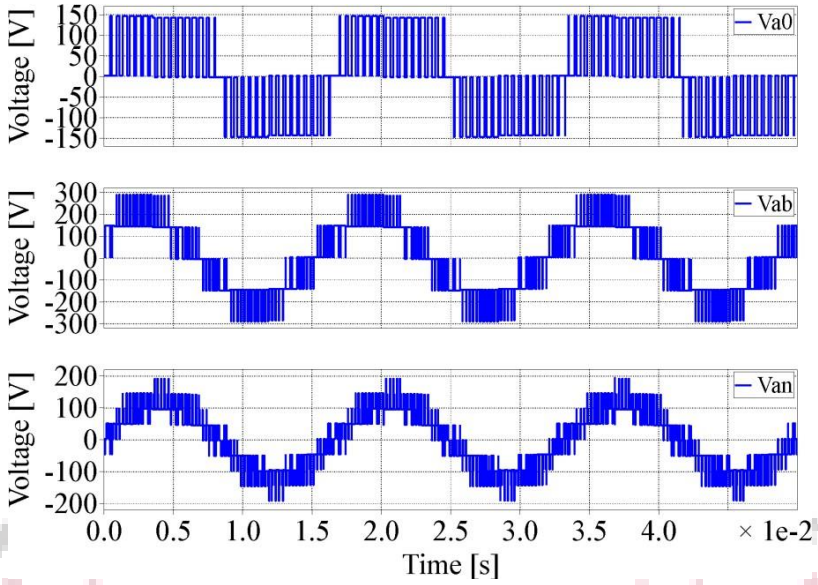

Figure 3.6: simulated time-domain waveforms of phase *a* pole voltage (top), v_{ab} line voltage (center), and phase *a* line-to-neutral voltage (bottom) using PD-SPWM.

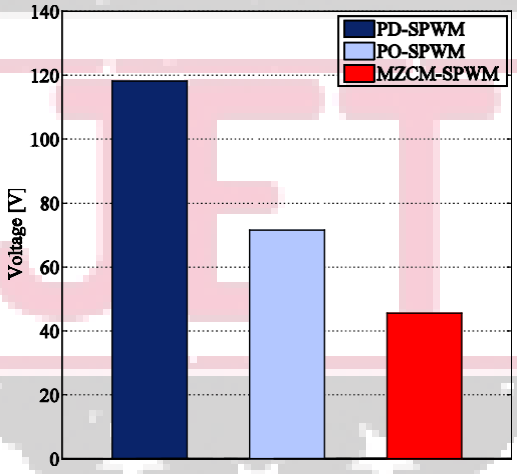

Figure 3.7: comparison of peak v_{ng} CMV generated by PD-, PO-, and MZCM-SPWM techniques.

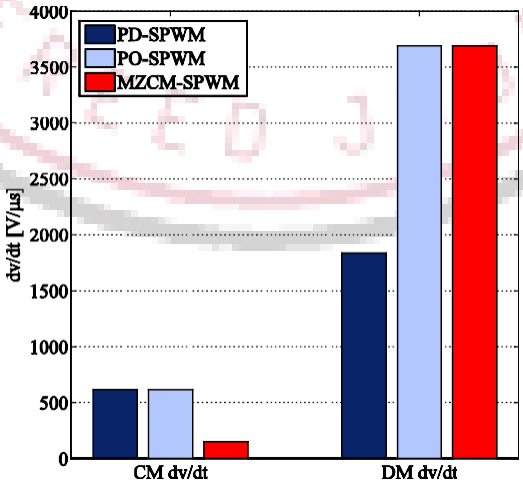

Figure 3.8: Comparison of CM and DM *dv/dt* generated by PD-, PO-, and ZCM-SPWM techniques.

IV. References

1. J. Pontt, J. Rodríguez, and R. Huerta, "Mitigation of noneliminated harmonics of SHEPWM three-level multipulse three-phase active front end converters with low switching frequency for meeting standard IEEE-519-92," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1594–1600, 2004.

2. D. A. Rendusara, E. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J. W. Gray, "Analysis of common mode voltage-"Neutral shift" in medium voltage PWM adjustable speed drive (MV-ASD) systems," *IEEE Transactions on Power Electronics*, vol. 15, no. 6, pp. 1124–1133, 2000.

3. J. Rodríguez, J. Pontt, P. Correa, P. Cortés, and C. Silva, "A new modulation method to reduce common-mode voltages in multilevel inverters," *IEEE Transactions on Industrial Electronics*, vol. 51, no. 4, pp. 834–839, 2004.

4. J. Rodríguez, J. Pontt, R. Huerta, and P. Newman, "24-pulse active front end rectifier with low switching frequency," in *Proceedings of the 35th IEEE Annual Power Electronics Specialists Conference (PESC '04)*, pp. 3517–3523, June 2004.

5. B. P. Schmitt and R. Sommer, "Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high-voltage IGBT based topology," in *Proceedings of the IEEE International Symposium on Industrial Electronics Proceedings (ISIE '01)*, pp. 746–751, June 2001.

6. F. Wang, "Motor shaft voltages and bearing currents and their reduction in multilevel medium-voltage PWM voltage-source-inverter drive applications," *IEEE Transactions on Industry Applications*, vol. 36, no. 5, pp. 1336–1341, 2000.

7. A. Videt, P. Le Moigne, N. Idir, P. Baudesson, and X. Cimetière, "A new carrier-based PWM providing common-mode-current reduction and DC-bus balancing for three-level inverters," *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 3001–3011, 2007.

8. F. Wang, "Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters," *IEEE Transactions on Industry Applications*, vol. 38, no. 2, pp. 500–506, 2002.

9. A. K. Gupta and A. M. Khambadkone, "A space vector modulation scheme to reduce common mode voltage for cascaded multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1672–1681, 2007.

10. R. S. Kanchan, P. N. Tekwani, and K. Gopakumar, "Three-level inverter scheme with common mode voltage elimination and dc link capacitor voltage balancing for an open-end winding induction motor drive," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1676–1683, 2006.

11. P. C. Loh, D. G. Holmes, Y. Fukuta, and T. A. Lipo, "A reduced common mode hysteresis current regulation strategy for multilevel inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 1, pp. 192–200, 2004.

12. P. K. Chaturvedi, S. Jain, and P. Agarwal, "A simple carrier based neutral point potential regulator for 3-level diode clamped inverter," *International Journal of Power Electronics*, vol. 3, no. 1, pp. 1–25, 2011.

13. P. K. Chaturvedi, S. Jain, and P. Agarwal, "Reduced switching loss pulse width modulation technique for three-level diode clamped inverter," *IET Power Electronics*, vol. 4, no. 4, pp. 393–399, 2011.

14. R. S. Kanchan, P. N. Tekwani, and K. Gopakumar, "Three-level inverter scheme with common mode voltage elimination and dc link capacitor voltage balancing for an open-end winding induction motor drive," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1676–1683, 2006.